REMARKS

Applicant would like to thank the Examiner for finding in the pending Office Action that Claims 2, 4, 7, 15, 20, 28, 30, & 33 recite allowable subject matter if rewritten to include the base independent claim and any intervening claims. Claims 1-38, 50, 51, and 53-56 are pending in this application. Applicant reserves the right to file continuing applications directed to the non-elected claims, Claims 39-49, 52, 59, and 60.

Telephonic Interview

Applicant acknowledges with appreciation the courtesies extended by the Examiner to Applicants representative in the telephonic interview conducted May 31, 2006. In the interview the bases for the rejection of the instant application under 35 U.S.C. § 102(b), 35 U.S.C § 102(e), and 35 U.S.C § 103 were discussed. The distinction between the Yamamoto and Devoe references and the present invention were recognized but no agreement was reached as to the language that would differentiate the present invention with those references. The Applicant submits that included in the present response will be a clear definition of terms which differentiate the invention from these references.

Objection to the Drawings

At page 2 of the pending Office Action, Examiner states that the drawings are objected to for failing to show every feature of the invention specified in the claims as required under 37 C.F.R. 1.83(a). Specifically, Examiner asserts that the claim language "resonant via is physically connected to only the first and second conducting pads" is not supported by the figures. In the telephonic interview conducted on May 31, 2006, Examiner noted that application Fig. 21, which depicts a plated through-hole embodiment of an internal "I" resonant via, comprises both "Capacitive Pads" and "Via Pads", where the former are the "first and second conducting pads" of the claims and the latter are incidental features of a through-hole structure. The currently amended

Claims 1, 10, and 23 renders this objection moot by replacing the objected to phrase with language that more accurately describes applicant's invention. Specifically, the claims as amended are intended to distinguish over prior art by limiting Applicant's invention to structures wherein the entire resonant via structure, including the via and first and second conducting pads plus any additional features such as the Via Pads of Fig. 21, forms a single physically isolated entity.

Accordingly, Applicant believes that Figs. 4 and 21 reasonably depict every required physical feature of corresponding claims 1, 10, & 23 as currently amended.

Rejection of Claims Under 35 U.S.C. § 102

The Law of Anticipation and Enabling Prior Art References

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. M.P.E.P. § 2131. The identical invention must be shown in as complete detail as is contained in the claim. *Id.*

Claims 1, 3, 5, 6, 8, and 9

At page 3 of the pending Office Action, Examiner rejects Claims 1, 3, 5, 6, 8, and 9 under 35 U.S.C. 102(b) as being anticipated by Yamamoto, et al. (U.S. Patent No. 5,451,917). Specifically, Examiner asserts that Fig. 6 of Yamamoto, et al. discloses every element of the above claims, including: first and second conducting planes (10, 11); a resonant via (6) physically connected to only the first and second conducting pads (4, 1); wherein the first and second conducting pads are located internally relative to the first and second conducting planes (10, 11). Applicant notes that element 1 of Fig. 6 is identified by Examiner as a conducting pad, whereas Yamamoto, et al. identify this element as a "lead line." A description of a lead line appears in Yamamoto, et al. at column 3, lines 14-18: "Formed in the signal layer LS that is located approximately at the center of the dielectric layers, the lead line 1 is a high-impedance line that is necessary for the choke circuit, to enable the passage of a

DC bias and refuse that of a high-frequency signal." It is clear from this and other portions of the written description, as well as depictions in the figures, including Fig. 6, that the lead line connects a DC voltage supply source at one location to semiconductor devices at other locations.

Lead line 1 in Fig. 6 is further physically connected to through-hole 6 to provide high frequency shunt capacitance to ground in order to accomplish the invention's purpose of shunting noise propagating within the lead line. Applicant's invention, in contrast, is directed to providing isolated resonant via structures for implementing a periodic stop band structure for blocking electromagnetic waves that only propagate within the dielectric medium between parallel conductors (the first and second conducting planes). Indeed, physically connecting the resonant via structures to each other or to other conducting entities would run counter to the intended operation of Applicant's invention.

The lead line disclosed by Yamamoto does not correspond to a conducting pad of Applicant's invention, the purpose of which is to increase the capacitive coupling of the attached via to a conducting plane. Applicant's pending claims pertain to isolated electrically conductive resonant structures that do not have a direct physical connections to any other electrical components of the system. Accordingly, independent Claim 1, 10, and 23 have been amended to more particularly point out and distinctly claim Applicant's invention and to clearly distinguish Applicant's invention over Yamamoto, et al.

Applicant respectfully submits that Claims 1, 3, 5, 6, 8, and 9 are patentable over Yamamoto, et al. and in condition for allowance.

Claims 1,3, 5, 6, 8-12 16, 18, 19, 21-26, 29, 31, 32, 34-38, 53, and 55

At page 4 of the pending Office Action, Examiner rejects Claims 1,3, 5, 6, 8-12 16, 18, 19, 21-26, 29, 31, 32, 34-38, 53, and 55 under 35 U.S.C. 102(e) as being anticipated by Devoe, et al. (U.S. Patent No. 6,542,352). Specifically, Examiner asserts that Fig. 16 of Devoe, et al. discloses every element of the above claims, including: first and second conducting planes (58); a plurality of vias (52) physically

connected to only the first and second conducting pads (54); wherein the first and second conducting pads are located internally relative to the first and second conducting planes (58). Examiner further notes "that each via 52 is a resonant via since each plated via inherently possesses inductance, and the capacitance is provided between the conducting pads 54 and the first and second conducting planes 58 (thus, providing a resonant shunt circuit) which will resonate at a predetermined frequency." In contrast, Devoe, et al. actually teaches away from including inductance in its capacitors such as those disclosed in their Fig. 16, etc. First, the equivalent schematic circuit for the structure displayed in Fig. 16 is simply two series capacitors without any inductors. Moreover, at column 3, lines 28-37, Devoe cites the importance of "low-inductance products since the speed of processors is increasing and voltages for processors are dropping to 2.2V." Thus, an objective of the Devoe structure of Fig. 16, etc. is to reduce inherent inductance in its capacitors to the lowest extent practicable. Applicant's objective on the other hand is quite the opposite; applicant's invention seeks to achieve by appropriate selection of inductance of the via (e.g., by choice of length and diameter) together with the appropriate selection of capacitance, to accomplish a resonant shunt circuit over a particular advantageous band of frequencies. Accordingly, independent Claims 1, 10, and 23 have been amended to distinctly claim this feature, which has abundant written description support.

Applicant specifically identifies the need for a prescribed inductance as an integral part of the resonant via in equation (3) at paragraph [41], which is a complex series formula for the shunt impedance of an array of wires (e.g., vias) in a TEM mode. And, paragraph [46] explicitly recites that the "inductance of a wire of length c in the wire media is given by $\frac{Z_s c}{j\omega b}$ where Z_s is given by equation (3) above." Note that "b" is the period in x and y and the dependence of inductance on via (wire) radius is included in equation (3). The dimension c is the height of the PPW for the mechanically-balanced resonant vias, and twice the height of the PPW for the mechanically-unbalanced resonant vias. This relationship to PPW height is clearly shown in Figure 16. The formula for inductance L is also presented in Figure 16 for

the limiting case where the via spacing (period) b is equal to or less than the electromagnetic wavelength. Thus, the written description abundantly discloses the factors that determine via inductance, including the relationship between via inductance and the period of the resonant vias, which enables a particular advantageous inductance of the vias to be selected *a priori*.

Applicant respectfully submits that Claims 1,3, 5, 6, 8-12 16, 18, 19, 21-26, 29, 31, 32, 34-38, 53, and 55 are patentable over Devoe and in condition for allowance.

Rejection of Claims Under 35 U.S.C. § 103

Claims 10-13, 16, 18, 19, 21, 22-26, 29, 31, 34-38, 50, 51, and 53

At page 5 of the pending Office Action, Examiner rejects Claims 10-13, 16, 18, 19, 21, 22-26, 29, 31, 34-38, 50, 51, and 53 under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto, et al. Specifically, Examiner asserts that it would have been obvious to one of ordinary skill in the art to provide more than one resonant via in Yamamoto's device "to attain more than one attenuation pole, or to obtain a desired filter frequency (e.g., stop band)." Applicant respectfully submits that Yamamoto, et al. does not disclose or suggest all the limitations of the above referenced claims. Yamamoto's device filters frequencies propagating within a conductive strip line wire, whereas Applicant's device filters electromagnetic waves propagating within a dielectric medium in a parallel plate waveguide. Yamamoto, et al. neither disclose nor suggests modifying their device to intercept and attenuate electromagnetic waves propagating through the dielectric medium as parallel-plate waveguide modes. Furthermore, they fail to provide the information necessary to enable one of ordinary skill in the art to accomplish any such modification.

Applicant respectfully submits that Claims 10-13, 16, 18, 19, 21, 22-26, 29, 31, 34-38, 50, 51, and 53 are patentable over Yamamoto and in condition for allowance.

Claims 14, 27, 50, 51, 54, and 56

At page 6 of the pending Office Action, Examiner rejects Claims 14, 27, 50, 51, 54, and 56 under 35 U.S.C. § 103(a) as being unpatentable over Devoe, et al. Specifically, Examiner asserts that it would have been obvious to one of ordinary skill in the art to provide resonant vias with spacing less than about one-half the wavelength of the desired stop band frequency. Devoe discloses at col. 18, lines 65-67 that "Other hole pitch and spacings are possible..." However, as with Yamamoto, et al., Devoe, et al. neither suggest nor contemplate employing their structures for the purpose of interacting with or attenuating electromagnetic waves propagating in the dielectric medium between parallel plates of a waveguide.

Applicant respectfully submits that Claims 14, 27, 50, 51, 54, and 56 are patentable over Devoe and in condition for allowance.

Conclusion

Applicant respectfully submits that all the pending claims, Claims 1-38, 50, 51, and 53-56, are patentable and in condition for allowance. Entry of these remarks and Amendment and further examination of the application are requested. A Notice of Allowance is solicited.

Respectfully submitted,
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